therefore the equivalent circuit shown in Figure 10.2-3e is valid. To turn the diode off it is necessary to remove all the excess minority-carrier charge stored on C_D. But this cannot be done instantaneously, and as long as there is any charge left on C_D, v_D will stay approximately equal to V_o and the diode will remain forward biased. Because the input voltage is now negative and the diode is still on, a large negative current flows out of the diode associated with the removal of the minority-carrier charge from C_D. Once this charge is completely removed, the diode enters the reverse-bias region and the equivalent illustrated in Figure 10.2-3b applies. As a result, at this point C_J now charges exponentially toward $-V_R$, and when C_J is fully charged, i_D will be zero and the diode will again be off.

In Figure 10.2-3f, t_{on}, t_s, and t_{rr} are known as the diode's on-time, storage time, and reverse recovery time, respectively. For a small-signal diode having square-wave input signal excitation, typical values for these switching parameters are $t_{on} = 7$ ns, $t_s = 700$ ns, and $t_{rr} = t_s + 4t_1 \simeq 700$ ns. These results indicate that the storage time usually dominates the transient response of a diode. A detailed analysis of this type of diode circuit is carried out in Problem 10.2-1.

10.2-2 Switching Characteristics of the Bipolar Junction Transistor

As with the *pn* junction diode, the large-signal switching performance of the BJT may be readily understood once the appropriate extensions of the small-signal models have been made. The small-signal hybrid-π transistor model is shown in Figure 6.4-4 and by examining this model you should recall that

$$r_{bb'} = \text{base spreading resistance} \tag{10.2-1a}$$

$$r_{b'e} = (1 + h_{fe})r_e \tag{10.2-1b}$$

$$r_e = \frac{V_T}{I_E}\left(\text{proportional to } \frac{1}{I_E}\right) \tag{10.2-1c}$$

$$C_{b'e} = C_{je} + C_{de} \tag{10.2-1d}$$

$$C_{je} = \text{emitter junction capacitance (a nonlinear function of } v_{B'E}) \tag{10.2-1e}$$

$$C_{de} = \text{emitter diffusion capacitance (proportional to } I_E) \tag{10.2-1f}$$

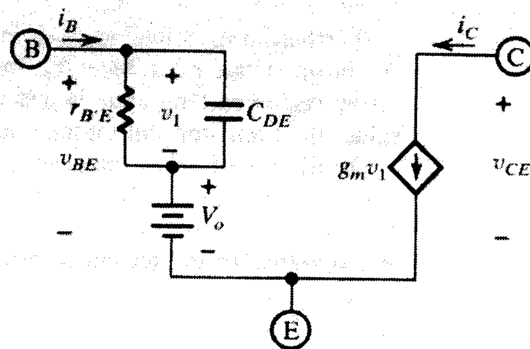
$$C_{b'c} = C_{jc} = \text{collector junction capacitance (a nonlinear function of } v_{CB'}) \tag{10.2-1g}$$

and

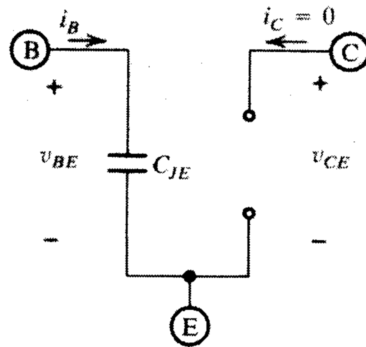
$$g_m = \frac{h_{fe}}{r_{b'e}} = \frac{h_{fe}}{(1 + h_{fe})r_e} \simeq \frac{I_E}{V_T} \text{ (proportional to } I_E) \tag{10.2-1h}$$

For simplicity, in extending this model to handle large signals, it will be convenient to consider that $r_{bb'} = 0$ and that $C_{b'c}$ is also zero. Nonzero values of $C_{b'c}$ may be handled by applying the Miller theorem (see Problem 10.2-7); however, in using this approach, we will need to assume that g_m is relatively constant even though it actually varies directly with I_E.

By setting $C_{b'c}$ and $r_{bb'}$ equal to zero, and including the voltage drop V_o across the base–emitter junction, we obtain the equivalent circuit shown in



(a) Approximate BJT Active-Region Large-Signal Model



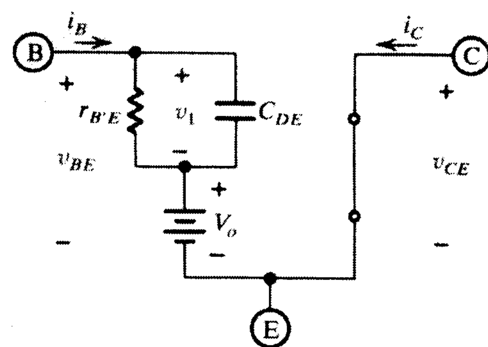


Figure 10.2-4
Approximate BJT large-signal models.

(b) BJT Large-Signal Model in Cutoff

(c) BJT Large-Signal Model in Saturation

Figure 10.2-4a. This is the equivalent circuit that we will use to represent the BJT when it is in the active region. Here $r_{B'E}$ is used to represent the average value of $r_{b'e}$ over all values between cutoff and saturation. In a similar fashion, C_{DE}, C_{JE}, and where needed, $r_{BB'}$ will also be used to represent the average values of C_{de}, C_{je}, and $r_{bb'}$, respectively. As with the diode, the junction capacitance C_{JE} has been neglected in comparison to the diffusion capacitance C_{DE} when the base–emitter junction is forward biased.

When the transistor is cut off, C_{JE} can no longer be neglected since C_{DE} is now nearly zero. Furthermore, in this region, with $I_E \approx 0$, the transistor g_m is also zero. Combining these facts, in cutoff the BJT model has the approximate form given in Figure 10.2-4b.

The model that is valid when the transistor saturates is essentially the same as that when it is active except that v_{CE} is nearly zero, and as a result this equivalent circuit has the form shown in Figure 10.2-4c. This representation is somewhat inaccurate since in reality, when the transistor saturates the effective time constant τ_s is different than τ_B, but in the interest of simplicity we use the same recombination time constant to represent the transistor's performance in both the active and saturation regions.

The overall switching performance of a BJT device in a given circuit is handled in much the same way as with the *pn* junction diode, by substituting in the appropriate model for the transistor and solving for the desired voltages and currents. As with the diode, the circuit components used in these models are considered to be constants in order to simplify the analysis.

Furthermore, as long as v_{BE} is less than V_o, the transistor will be assumed to be cut off. Once v_{BE} reaches V_o, the transistor will be considered to be in the active region as long as i_C is less than $I_{C,\text{sat}}$. Once i_C attempts to exceed this value, the transistor will saturate, and the model in Figure 10.2-4c will apply.

To illustrate how to calculate the important switching times for the bipolar junction transistor, let's carefully examine the circuit illustrated in Figure 10.2-5a. In carrying out a quantitative analysis of this circuit, we will make extensive use of the technique presented in Appendix I.5 regarding the transient analysis of simple RC networks by inspection. If you have forgotten how to do this, you should reread this material, paying particular attention to equation (I.5-1). In analyzing this circuit we will assume that the models given in Figure 10.2-4 may be used to represent the transistor. In addition, V_F and V_R will be considered to be much larger than V_o, so that V_o may be neglected and switching between active and cutoff can be assumed to take place at $v_{BE} = 0$.

If we consider that the input voltage has been equal to $-V_R$ for a long time, the transistor will initially be cut off, and at $t = 0-$ the model in Figure 10.2-5b will apply with $v_{BE}(0-) = -V_R$, $i_C(0-) = 0$, and $v_{CE}(0-) = V_{CC}$. At $t = 0$ the input signal changes to $+V_F$, but because the junction capacitance cannot charge instantaneously, the transistor remains off (for a while at least), the equivalent circuit in Figure 10.2-5c applies, and at $t = 0+$ we have

$$v_{BE}(0+) = v_{BE}(0-) = -V_R \tag{10.2-2a}$$

and

$$i_B(0+) = \frac{V_F - v_{BE}(0+)}{R_B} = \frac{V_F + V_R}{R_B} \tag{10.2-2b}$$

Using equation (I.5-1), we may write down $v_{BE}(t)$ and $i_B(t)$ by inspection as

$$v_{BE}(t) = \underbrace{-V_R}_{\text{initial value}}e^{-t/\tau_1} + \underbrace{V_F}_{\text{final value}}(1 - e^{-t/\tau_1}) \tag{10.2-3a}$$

and

$$i_B(t) = \frac{V_F + V_R}{R_B}e^{-t/\tau_1} \tag{10.2-3b}$$

These waveshapes are sketched in Figure 10.2-5d.

All during the time that v_{BE} is less than zero (actually V_o) volts, the transistor is cut off, and $i_C = 0$ and $v_{CE} = V_{CC}$. The time required for C_{JE} to charge all the way up to zero volts is called t_d, the transistor's delay time. Strictly speaking, t_d is actually defined as the time needed after the switching occurs

Figure 10.2-5
Large-signal switching performance of a BJT.

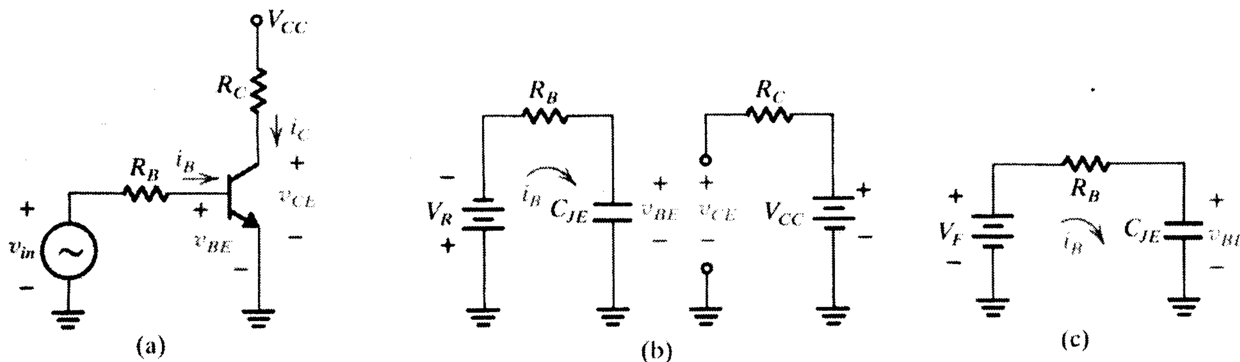
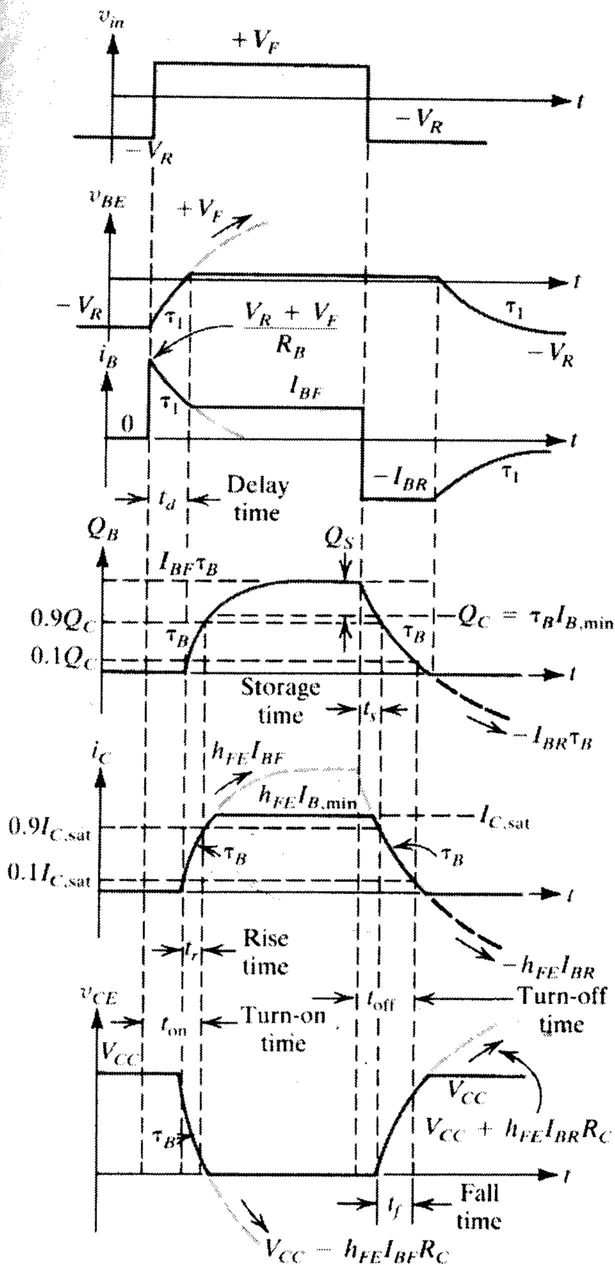
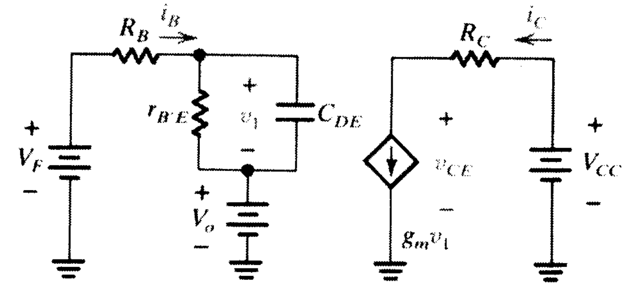
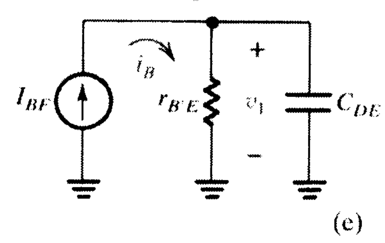


Figure 10.2-5 (continued)

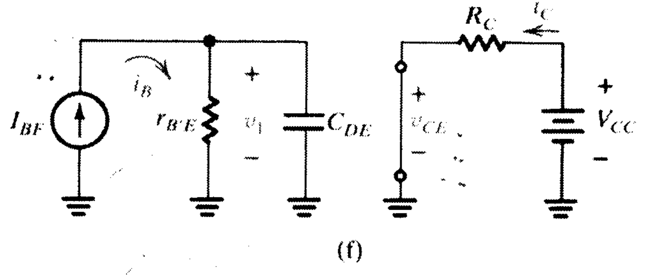


(d)

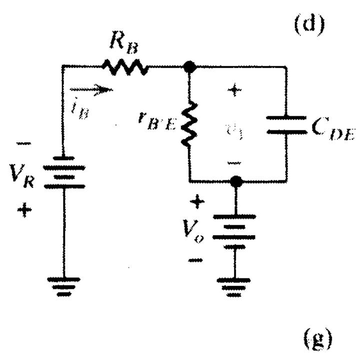


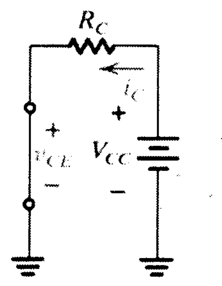


(e)

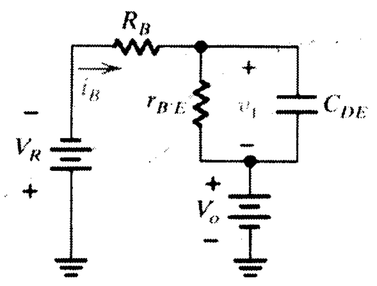


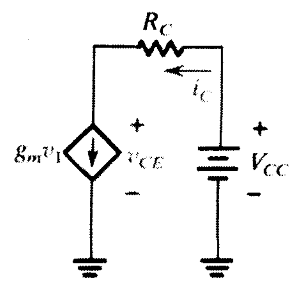
(f)





(g)





(h)

for i_C to reach 10% of its final value; but for simplicity, we approximate it as the time required for the transistor to just turn ON. Using this approximation for t_d, this time interval may be found by setting v_{BE} equal to zero in equation (10.2-3a) and solving for t. Carrying out this procedure, we obtain

$$t_d = \tau_1 \ln \frac{V_F + V_R}{V_F} \tag{10.2-4a}$$

where
$$\tau_1 = R_B C_{JE} \tag{10.2-4b}$$

When v_{BE} reaches zero the active model presented in Figure 10.2-5e applies, and assuming that R_B is much greater than $r_{B'E}$,

$$i_B \simeq \frac{V_F - V_o}{R_B} \simeq \frac{V_F}{R_B} = I_{BF} \tag{10.2-5a}$$

and
$$v_1(t) = I_{BF} r_{B'E}(1 - e^{-t/\tau_B}) \tag{10.2-5b}$$

where
$$\tau_B = r_{B'E} C_{DE} \tag{10.2-5c}$$

The quantity τ_B is a fundamental transistor parameter known as the minority-carrier lifetime in the base and is similar to the recombination time τ_r in diodes. By using equation (6.4-33b), it is not too difficult to show that τ_B can also be written as

$$\tau_B = \frac{1}{2\pi f_B} = \frac{1 + h_{FE}}{2\pi f_T} \tag{10.2-5d}$$

where f_T is the common-emitter unity-gain crossover frequency.

With the transistor now operating in the active region, the collector current may be written as

$$i_C(t) = g_m v_1(t) = g_m r_{B'E} I_{BF}(1 - e^{-t/\tau_B}) \tag{10.2-6a}$$

By using equation (10.2-1h) and substituting $h_{FE}/r_{B'E}$ for g_m, this expression reduces to the more familiar form

$$i_C(t) = h_{FE} I_{BF}(1 - e^{-t/\tau_B}) \tag{10.2-6b}$$

In addition, the collector-to-emitter voltage may also be written as

$$v_{CE}(t) = V_{CC} - i_C R_C = V_{CC} - h_{FE} I_{BF} R_C(1 - e^{-t/\tau_B}) \tag{10.2-7}$$

If I_{BF} is greater than $I_{B,\min}$, the transistor will saturate before the collector current reaches the final value predicted by equation (10.2-6b). When this occurs, as illustrated in Figure 10.2-5d, the collector current will flatten out at $I_{C,\text{sat}}$, and v_{CE} will also flatten off at zero.

The charge on C_{DE}, which is equal to the excess minority carrier charge stored in the base, is given by

$$Q_B(t) = C_{DE} v_1(t) = I_{BF} \tau_B(1 - e^{-t/\tau_B}) \tag{10.2-8a}$$

and for reasons that will be apparent shortly, it is also convenient to note that this expression for the base charge can be rewritten using equation (10.2-6b) as

$$Q_B(t) = \frac{\tau_B}{h_{FE}} h_{FE} I_{BF}(1 - e^{-t/\tau_B}) = \frac{\tau_B}{h_{FE}} i_C(t) \tag{10.2-8b}$$

As the base charge increases (if $I_{BF} > I_{B,\min}$), the transistor will eventually saturate. This will occur when the collector current level is

$$i_C = I_{C,\text{sat}} \simeq \frac{V_{CC}}{R_C} \tag{10.2-9a}$$

and

$$i_B = I_{B,\min} = \frac{I_{C,\text{sat}}}{h_{FE}} \tag{10.2-9b}$$

The corresponding minority-carrier charge stored in the base at this point is given by equation (10.2-8b) as

$$Q_c = \frac{\tau_B I_{C,\text{sat}}}{h_{FE}} = \frac{\tau_B h_{FE} I_{B,\min}}{h_{FE}} = \tau_B I_{B,\min} \tag{10.2-9c}$$

The transistor rise time, or the time for the transistor collector current to go from 10% to 90% of its final value, may be determined by using equation (10.2-6b) to find the times required for $i_C(t)$ to reach 0.1 and $0.9 I_{C,\text{sat}}$, setting their difference equal to t_r. Carrying out this procedure, we obtain

$$t_r = \tau_B \ln \frac{I_{BF} - 0.1 I_{B,\min}}{I_{BF} - 0.9 I_{B,\min}} \tag{10.2-10}$$

The sum of t_d and t_r is known as the transistor turn-on time, t_{on}.

After the transistor saturates, although i_C flattens off at $I_{C,\text{sat}}$, following the equivalent circuit in Figure 10.2-5f, we find that C_{DE} continues to charge toward $I_{BF}\tau_B$. The additional charge added beyond Q_c is called the storage charge (Q_s), and later when we try to turn the transistor off, we will see that all of this charge must be removed from the base before the transistor can come out of saturation.

When v_{in} switches to $-V_R$, the equivalent circuit shown in Figure 10.2-5g applies until all the storage charge Q_s is removed from the base. If $R_B >> r_{B'E}$ and also if $V_R >> V_o$, then here

$$i_B = \frac{V_o - V_R}{R_B} \simeq \frac{-V_R}{R_B} = -I_{BR} \tag{10.2-11a}$$

Thus

$$v_1(t) = I_{BF} e^{-t/\tau_B} - I_{BR} r_{B'E}(1 - e^{-t/\tau_B}) \tag{10.2-11b}$$

and

$$Q_B(t) = C_{DE} v_1 = I_{BF}\tau_B e^{-t/\tau_B} - I_{BR}\tau_B(1 - e^{-t/\tau_B}) \tag{10.2-11c}$$

redefining $t = 0$ as the point where v_{in} switches to $-V_R$. The time required to reduce $Q_B(t)$ to 90% of Q_c is called t_s, the storage time. Following equation (10.2-9c), we may write

$$Q_B(t_s) = 0.9Q_c = 0.9\tau_B I_{B,\min} = I_{BF}\tau_B e^{-t_s/\tau_B} - I_{BR}\tau_B(1 - e^{-t_s/\tau_B}) \tag{10.2-12a}$$

and solving this expression for t_s, we have

$$t_s = \tau_B \ln \frac{I_{BR} + I_{BF}}{I_{BR} + 0.9 I_{B,\min}} \tag{10.2-12b}$$

After all the storage charge is removed, the transistor comes out of saturation, reenters the active region, and the equivalent circuit given in Figure 10.2-5h applies. Because the input circuit has not changed, $i_B(t)$, $v_1(t)$, and $Q_B(t)$ are still given by equations (10.2-11a), (10.2-11b), and (10.2-11c), respectively.

Therefore, because the transistor is now active, collector current and collector-to-emitter voltage may be immediately written as

$$i_C(t) = g_m v_1 = h_{FE} I_{B,\min} e^{-t/\tau_B} - h_{FE} I_{BR}(1 - e^{-t/\tau_B}) \tag{10.2-13a}$$

and

$$v_{CE}(t) = V_{CC} - i_C R_C = V_{CC} - h_{FE} R_C[I_{B,\min} e^{-t/\tau_B} - I_{BR}(1 - e^{-t/\tau_B})] \tag{10.2-13b}$$

The decrease in collector current predicted by equation (10.2-13a) continues until $Q_B(t)$ [or, alternatively, $i_C(t)$] reaches zero. At this point the base–emitter junction goes off and the transistor enters cutoff. Starting at the point where the transistor reenters the active region, and calling this point $t = 0$, the expressions for the $Q_B(t)$ and $i_C(t)$ may now be written as

$$Q_B(t) = I_{B,\min} \tau_B e^{-t/\tau_B} - I_{BR} \tau_B(1 - e^{-t/\tau_B}) \tag{10.2-14a}$$

and

$$i_C(t) = h_{FE} I_{B,\min} e^{-t/\tau_B} - h_{FE} I_{BR}(1 - e^{-t/\tau_B}) \tag{10.2-14b}$$

The transistor fall time, or the time for the transistor collector current to go from 90% to 10% of $I_{C,\text{sat}}$, may be determined by using equation (10.2-14b) to find the times required for $i_C(t)$ to reach 0.9 and $0.1 I_{C,\text{sat}}$, setting their difference equal to t_f. Carrying out this procedure, we obtain

$$t_f = \tau_B \ln \frac{I_{BR} + 0.9 I_{B,\min}}{I_{BR} + 0.1 I_{B,\min}} \tag{10.2-15}$$

The sum of the storage and fall times is known as the turn-off time, t_{off}, of the transistor.

Once $Q_B(t)$ reaches zero, the base–emitter junction is reversed biased, and the circuit model in Figure 10.2-5b again applies. In this region $i_C = 0$ and $v_{CE} = V_{CC}$. In addition, because the initial voltage on the capacitor is $v_{BE}(0+) = 0$ [defining $t = 0$ as the point at which the transistor just cuts off], we may write

$$v_{BE}(t) = -V_R(1 - e^{-t/\tau_1}) \tag{10.2-16a}$$

and

$$i_B(t) = \frac{-V_R}{R_B} e^{-t/\tau_1} \tag{10.2-16b}$$

Of course, the recovery of these voltage and current waveshapes takes about $4\tau_1$ (Figure 10.2-5d).

10.2-3 Switching Characteristics of the Field-Effect Transistor

The basic FET switching problem is illustrated in Figure 10.2-6a. Here C_{gs} and C_{gd} are the parasitic capacitances of the FET and C_L represents the combination of the transistor drain-to-source capacitance and any stray capacitance associated with the wiring or the next stage connected onto the transistor.

For the JFET you should recall that C_{gs} and C_{gd} are nonlinear functions of the voltage between the gate and the channel, while for the MOSFET these capacitances are relatively constant. In addition, for both MOSFETs and JFETs the drain current is nonlinearly related to the gate-to-source voltage (see, e.g., Figure 10.2-6b). These nonlinearities make it difficult to analyze the transient

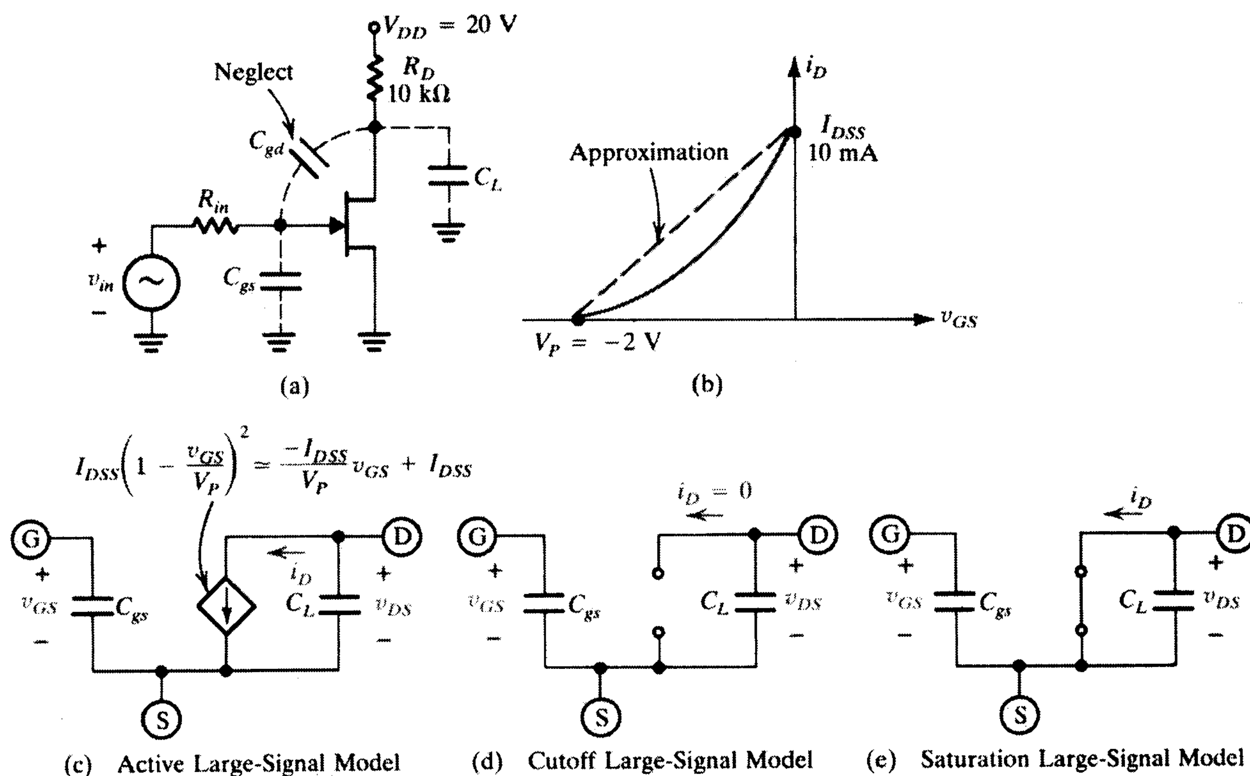


Figure 10.2-6
Large-signal FET models.

large-signal switching performance of FETs, and therefore to simplify this investigation, the following assumptions will be made:

1. The parasitic capacitances are constants independent of the transistor voltages.
2. The Miller feedback capacitance, C_{gd}, is negligible. This capacitance can easily be included later by applying the Miller theorem (see Problem 10.2-10).
3. The transistor g_m is a constant independent of v_{GS}. This is equivalent to saying that the i_D versus v_{GS} curve may be approximated by a straight line (see the dashed line in Figure 10.2-6b).

In addition, and again to ease the mathematical details, two more simplifying approximations will also be made:

4. The power supply voltage V_{DD} is much greater than the magnitude of the pinch-off voltage, V_p, and as a result, when the transistor enters the ohmic region, we may consider that v_{DS} is nearly zero.
5. The input and output time constants are widely separated from one another, so that the shorter of the two can be ignored.

Using these approximations, the transient analysis of the field-effect transistor is quite straightforward, and the equivalent circuits given in Figure 10.2-6c, d, and e are seen to represent the FET when it is active, cutoff, and saturated, respectively. In the example that follows we examine the FET switching

circuit illustrated in Figure 10.2-6a for the case where $C_L >> C_{gs}$. The opposite situation, namely th t where $C_{gs} >> C_L$, is left as an exercise for the homework (Problem 10 2-10).

EXAMPLE 10.2-1

The transistor in the switching circuit in Figure 10.2-6a has the i_D versus v_{GS} characteristics shown in part (b) of the figure. In addition, C_L = 15 pF and C_{gs} is so small that it may be neglected. If v_{in} is a 500-ns-wide periodic pulse train switching between 0 and −10 V, sketch v_{GS}, i_D, and v_{DS}.

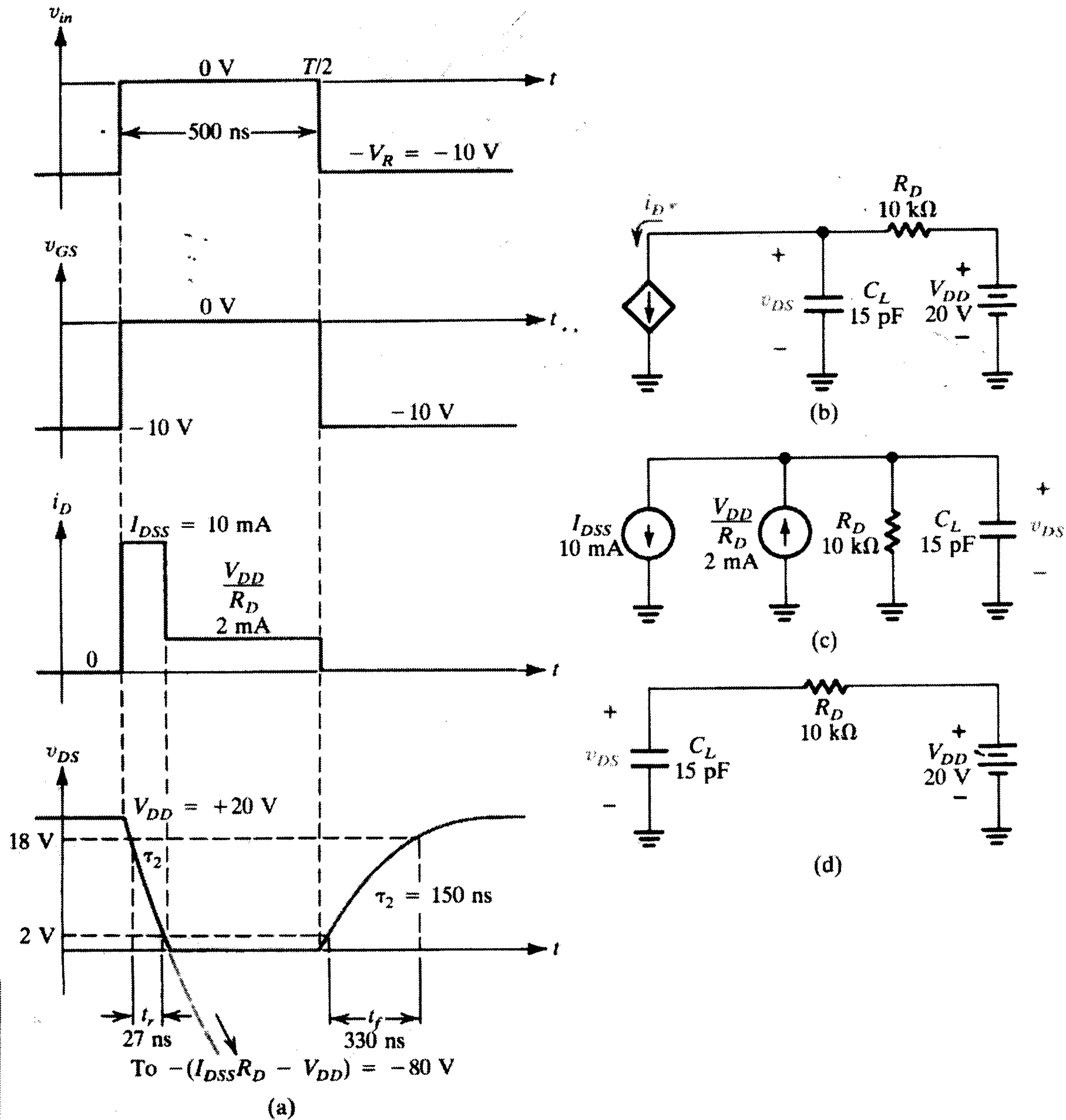


Figure 10.2-7
Example 10.2-1.

SOLUTION

For this case, with $C_{gs} = 0$, v_{GS} follows v_{in} (see Figure 10.2-7a). The basic form of the output equivalent circuit is illustrated in part (b) of the figure. If we assume that the period of the switching signal v_{in} allows sufficient time for the circuit waveshapes to reach steady state, then at $t = 0-$ with $v_{in} = -V_R$ just before it switches to zero, $v_{DS}(0-) = V_{DD}$.

When v_{in} switches to zero, i_D jumps up to I_{DSS} and the output equivalent circuit is given by Figure 10.2-7c (after a Thévenin-to-Norton transformation has been made). By inspection of this circuit, the drain-to-source voltage is seen to be

$$v_{DS}(t) = V_{DD}e^{-t/\tau_2} - (I_{DSS}R_D - V_{DD})(1 - e^{-t/\tau_2}) \qquad (10.2\text{-}17)$$

with $\tau_2 = R_D C_L$, so that the circuit rise time (or turn-on time) is given by

$$t_r = \tau_2 \ln \frac{I_{DSS}R_D - 0.1V_{DD}}{I_{DSS}R_D - 0.9V_{DD}} \simeq 27 \text{ ns} \qquad (10.2\text{-}18)$$

Once v_{DS} reaches zero, the transistor enters the ohmic region, and to the extent that we can neglect the transistor ON resistance, i_D immediately drops to $V_{DD}/R_D = 2$ mA.

At $t = T$ when the input switches from zero to $-V_R$ volts, the transistor cuts off and the drain current immediately goes to zero. The output equivalent circuit during this interval is that given in Figure 10.2-7d. If we redefine $t = 0$ at this switching point, and note that $v_{DS}(0-) = 0$ for this circuit, it immediately follows that

$$v_{DS}(t) = V_{DD}(1 - e^{-t/\tau_2}) \qquad (10.2\text{-}19)$$

Thus the waveshape for $v_{DS}(t)$ in this region is a full exponential and the fall time is therefore about $2.2\tau_2$, or 330 ns, while the turn-off time (or time for v_{DS} to reach 90% of its final value) is equal to $2.3\tau_2$ or about 345 ns for this particular circuit.

Exercises

10.2-1 For the circuit in Figure 10.2-3a, v_{in} is a 2-V(p-p) square wave, $C_J = 10$ pF, and $\tau_r = 1\ \mu$s. Determine the diode turn-on time if $R = 1$ kΩ. (*Note:* Because the signal amplitude is small, the 0.7-V diode drop cannot be neglected.) ***Answer*** 19 ns

10.2-2 Determine the diode storage time for the circuit described in Exercise 10.2-1. ***Answer*** 163 ns

10.2-3 The parameters for the BJT in the circuit in Figure 10.2-5a are $h_{FE} = 20$, $C_{JE} = 20$ pF, and $\tau_B = 100$ ns. If $R_B = 10$ kΩ, $R_C = 2$ kΩ, and $V_{CC} = 10$ V, find the time required for v_{CE} to reach 0.2 V when v_{in} changes from 0 to 5 V. ***Answer*** 114 ns